New Operational Mode of Diode Clamped Multilevel Inverters for Pure Sinusoidal Output

Jawad Ali, Muhammad Iftikhar Khan, Khadim Ullah Jan

Abstract—A new operational mode for diode clamped multilevel inverters (DCMLI) based on 5-level operation is proposed. This operational mode is based on a new technique called sinusoidal pulse width modulation (SPWM). Such operation aims to avoid the imbalance problem of the DC-link capacitors for multilevel inverters with more than 3-levels. This scheme reduces the DC-link capacitance without introducing any significant voltage ripple at the DC-link nodes. The proposed scheme can be generalized for any number of levels. Validity of the proposed operational mode of multilevel inverter is confirmed by simulations on a prototype 5-level DCMLI using MATLAB®.

Index Terms—5-level operation, diode clamped inverters, multilevel inverters, PWM, sinusoidal output, switching circuits

1 Introduction

Electrical appliances varies from low to medium and medium to high voltage applications, such as power tools, microwaves, TVs and audio/video equipments. Since main part of these appliances work on AC, thus it needs to be produced continuously. One of the building blocks of power electronics switches that have played a significant role in this view is "*inverter*". The main function of the inverters is to generate from one or multiple DC sources an AC output waveform, with amendable phase, frequency, and amplitude to meet the requirements of a particular application. Inverters applications includes power-switching supplies, uninterruptable power supplies (UPS), and linear power supplies. All of these utilize the DC-AC power inverters.

The inverter with output voltage of 3-level or more is referred as multilevel inverter. Fundamentals of a new diode clamping multilevel inverter have been discussed in full detail in [1]. Bouhali et al. [2] developed DC-link capacitor for voltage balancing in a 3-phase diode clamped inverter controlled by a direct space vector of line to line voltages. Shukla et al. [3] introduced control schemes for DC capacitor voltages equalization in diode clamped multilevel inverter (DCMLI) based DSTATCOM. Monge et al. [4] proposed multilevel diode clamped converter for photovoltaic (PV) generators, with independent voltage control of each solar array. Renge and Suryawanshi [5] developed 5-level diode clamped inverter to eliminate common mode voltage and reduced dv/dt in medium voltage rating induction motor drives. Hideaki Fujita and Naoya Yamashita [6] discussed performance of a diode clamped linear amplifier. Hatti et al. [7] proposed a 6.6-kV transformer less motor drive using a 5-level diode clamped pulse width modulation (PWM) inverter for energy savings of pumps and blowers. Srinivas in [8] discussed uniform overlapped multi carrier PWM technique. Ozdemir et al. [9] introduced fundamental frequency modulated 6-level DCMLI for 3-phase standalone PV system. Berrezzek Farid and Omeiri Amar [10] carried out a study on new techniques of controlled PWM inverters. Shukla et al. [11] proposed flying capacitor based chopper for DC capacitor voltage balancing in DCMLI.

This paper discusses a new operational mode for enhanced pure sinusoidal output voltage of a 5-level DCMLI using sinusoidal PWM (SPWM). Arrangement of remaining paper is: Part 2 provides a comprehensive discussion on multilevel inverter operation. In Part 3 the technique of SPWM is discussed in detail along with a comparison between filtered and unfiltered output voltages.

2 Multilevel Inverters Operation

The general structure of multilevel inverters is to produce sinusoidal output voltage from various levels of voltages obtained from capacitor voltage sources. The term multilevel starts from 3-levels. A 3-level inverter is also called multilevel inverter having two capacitor voltages in series. Due to the centre tap as neutral, such inverters are also known as neutral-clamped inverter. Each phase part of 3-level inverter has two pair of switching devices in series and the centre of each pair is clamped to the neutral through clamping diode. Multilevel inverter has become the most effective and practical solution for increasing power and reducing harmonic distortion for AC loads. Multilevel inverters are classified into three categories namely diode clamped inverters, flying capacitor inverters and cascaded inverters. In 3-phase multilevel inverters the number of main switches for each category is same. As Compared to other components numbers, for example clamping diodes and DC-link capacitors have the same capacity per unit. DCMLI needs least number of capacitors than other two topologies, but it requires additional clamping diodes. Flying capacitor inverter requires more capacitors, thus cascaded inverters are considered to be the simplest structure. DCMLI uses the mechanism of diodes to limit voltage stresses on power devices [12]. DCMLI usually consists of (m-1) capacitors on the DC bus, where "m" is the total number of negative, zero, and positive levels in the output voltage.

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Fig. 1-(a, b) shows a 3-phase half-bridge 5-level DCMLI. The order of numbering of the switches for phase "*a*" is S_1, S_2, S_3, S_4, S_5, S_6, S_7, and S_8 likewise for other two phases as well.

The DC bus consists of four capacitors C_1, C_2, C_3 and C_4 acting as voltage divider. For a DC bus voltage V_{DC}, the voltage across each capacitor is $V_{DC}/4$ and voltage stress on each device is limited to $V_{DC}/4$ through clamping diode. The principle of diode clamping to DC-link voltages can be extended to any number of voltage levels. The voltages across the semiconductor switches are limited by conduction of the diodes connected to various DC levels. Due to such arrangement of diodes, this class of multilevel inverter is termed as DCMLI. Table 1 shows the output voltage levels and the corresponding switch states for 1-phase "*a*" of the chosen 5-levels DCMLI.

As shown in Fig. 1-(a) the switches are arranged into four pairs as (S_1, S_5), (S_2, S_6), (S_3, S_7) and (S_4, S_8). If one of the switches in a pair is turned ON, the complementary switch of the same pair must be OFF. Four switches may be triggered at any time to select the desired level in the 5-level DCMLI. Four switches may be triggered at any time to select the desired level in the 5-level DCMLI.

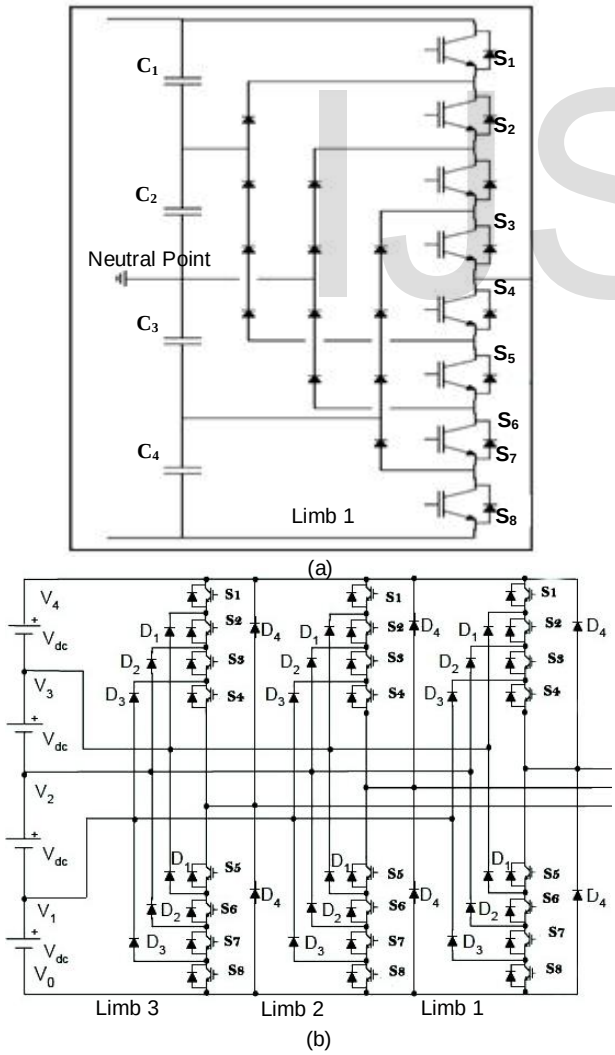

Fig. 1. 3-phase 5-level DCMLI (a) one leg (b) three legs

TABLE 1.
SWITCHING SCHEME FOR 1-PHASE OF A 3-PHASE 5-LEVEL DCMLI

Switching Scheme Configurations for Phase "*a*"

	Output Voltage	Switch Configurations							
S. No	V_o	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1.	$V_{DC}/2$	1	1	1	1	0	0	0	0
2.	$V_{DC}/4$	0	1	1	1	1	0	0	0
3.	0	0	0	1	1	1	1	0	0
4.	$-V_{DC}/4$	0	0	0	1	1	1	1	0
5.	$-V_{DC}/2$	0	0	0	0	1	1	1	1

The steps involved in producing 5-level 1-phase output voltage in this work are as mentioned below.

1. For phase "*a*" output voltage that corresponds V_o=0, two upper switches S_3, S_4 and two lower switches S_5 and S_6 are turned ON.
2. For an output voltage of $V_o=V_{DC}/4$, three upper switches S_2, S_3, S_4 and one lower switch S_5 is turned ON.
3. For an output voltage of $V_o=V_{DC}/2$, all upper switches S_1 through S_4 are turned ON and S_5 to S_8 are OFF.
4. For output voltage of $V_o= -V_{DC}/4$, upper switch S_4 and three lower switches S_5, S_6 and S_7 are turned ON.
5. To obtain the output voltage of $V_o= -V_{DC}/2$, all the four lower switches S_5, S_6, S_7 and S_8 are turned ON.

The same procedure is used for other two phases of DCMLI.

3 SINUSOIDAL PULSE WITH MODULATION (PWM) TECHNIQUES

To produce output voltage in multilevel inverters, the duty cycle of switches can be cleared by using special PWM techniques. Due to this fact, a proper switching transition is chosen using a controller to construct the most wanted output voltage. In this work a newly introduced technique namely SPWM is used to supply gate signals to these power switches.

All switches of the three legs are based upon working in complementary mode. Each inverter leg has its own binary gate signal, which is used to control that picky inverter leg. In SPWM, generation of the preferred output voltage is achieved by comparing the desired sinusoidal reference waveform (modulating signal) with a high frequency triangular "*carrier*" wave using MATLAB® SIMULINK Toolbox. The whole scenario of SPWM generated output waveform and arrangement of various limbs in SIMULINK Toolbox is as shown in Fig. 2 and Fig. 3 respectively.

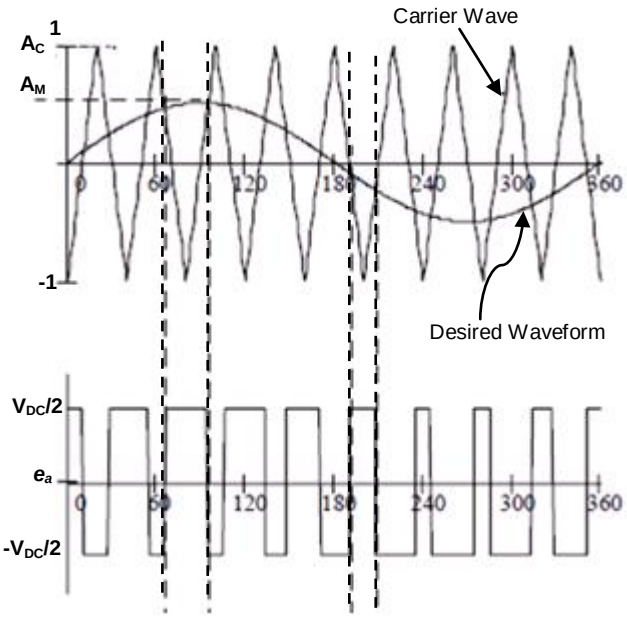

Fig. 2. Sinusoidal pulse width modulation generation

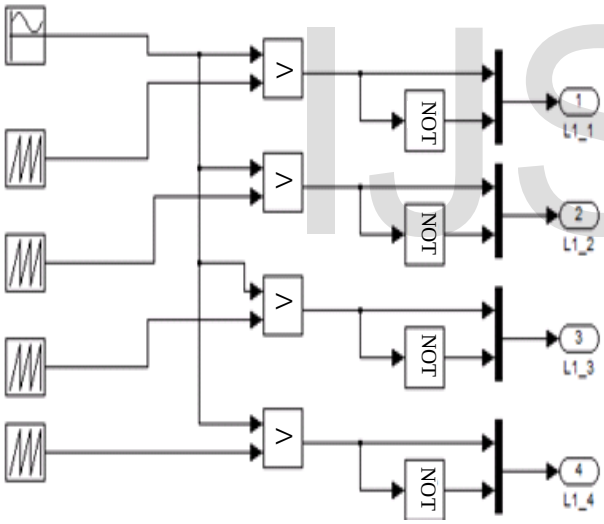

Fig. 3. Internal circuitry of the main subsystem/model using SIMULINK®
(5-level diode clamped inverter)

This block provides control signals for all the eight power switches (MOSFET) on the first leg of 3-phase 5-level diode clamped inverter. The block in Fig. 3 consists of four relational operators. Each relational operator will make a comparison between two signals (high frequency triangular carrier waveform and the reference modulating signal) producing only one output signal. Since it is clearly indicated in the Fig. 3 "Limb 1'' that two signals are compared using relational operator, which acts like a comparator. It compares the modulating sinusoidal signal and the triangular carrier signal given at its input part.

It is seen that when the voltage of the sinusoidal wave becomes larger than the high frequency carrier signal, the output of the relational operator (comparator) will output logic "1", on the other hand if the voltage of the modulating sinusoidal signal is lower than the high frequency triangular carrier signal then the relational operator will output logic "0". In order to obtain zero output voltage, a NOT gate is installed in front of the original output of the relational operator. The original output is fed to the NOT gate, which changes the input value to its complement state (zero output). This results in another output signal which is a compliment value of the original output of the relational operator. As it can be observed in Fig. 3 that outputs of the relational operator and NOT gate are then fed to a multiplexer which combines these two unlike signals into one output signal.

Each of the four relational operators (comparators) performs the same function. In short block "Limb 1" provides four composite signals and for these signals there are four de-multiplexers installed inside block named *'5- level diode clamped'* as indicated in Fig. 3. The other blocks "Limb 2" and "Limb 3" performs exactly the same function as of the block "Limb 1" for the remaining inverter legs L_2 and L_3 respectively.

As shown in Fig. 1-(a) each leg of the 3-phase 5-level diode clamped inverter has twelve clamping diodes and eight power switching devices such as MOSFETs. All leg voltage waveforms consist of five different voltage levels in the staircase arrangement. These waveforms have been plotted and shown in Fig. 4.

It is observed in Fig. 4 that each leg voltage actually consists of five different steps or voltage levels. These voltage levels are in steps of "0", "100", "200", "-100" and "-200" volts for the leg voltage $V_{an}(t)$. The other two legs will produce a voltage waveform that will be similar in construction like $V_{an}(t)$. All the waveforms will have different values of voltage levels or step size. In general these leg voltages are represented as $V_{an}(t)$, $V_{bn}(t)$ and $V_{cn}(t)$ for legs L_1, L_2, and L_3 respectively.

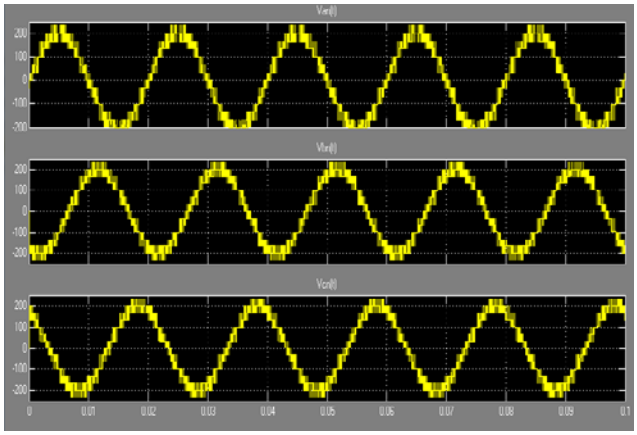

Fig. 4. Leg voltages of the 3-phase 5-level diode clamped inverter

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Frequency ratio plays an important role in PWM techniques. It is defined as *"the ratio of the carrier signal frequency to the frequency of the modulating signal"*. The higher ratio indicates a more sinusoidal output current. It determines the number of pulses, during each cycle in the output voltage of the inverter.

$K_f = f_c/f$ ……Eq. (1)

where "f_c" and "f" are called the frequencies of the carrier and modulating signals respectively.

The line voltages can be obtained in the following order.

$V_{ab}(t) = V_{an}(t) - V_{bn}(t)$ ……Eq. (2)

$V_{bc}(t) = V_{bn}(t) - V_{cn}(t)$ ……Eq. (3)

$V_{ca}(t) = V_{cn}(t) - V_{an}(t)$ ……Eq. (4)

In order to increase the performance capability and efficiency of 3-phase 5-level diode clamped inverter, it is essential that the inverter can produce output line voltages with less or negligible contents of harmonic components. There are several ways to reduce the harmonics from the unfiltered output line voltages. To ensure brevity only three of these schemes are listed and discussed comprehensively.

- Appropriate choice of the switching angles
- Increased number of power switching devices or the number of voltage levels/steps
- Using filter circuit

It should be kept in mind that the switching angles must be properly and accurately calculated for each of the power switching devices namely (S_1, S_2…S_8). The carefull selection of such angles ensures the harmonic elimination in the output voltage that enhances the utility of the inverter circuit and makes the inverter to work more efficiently.

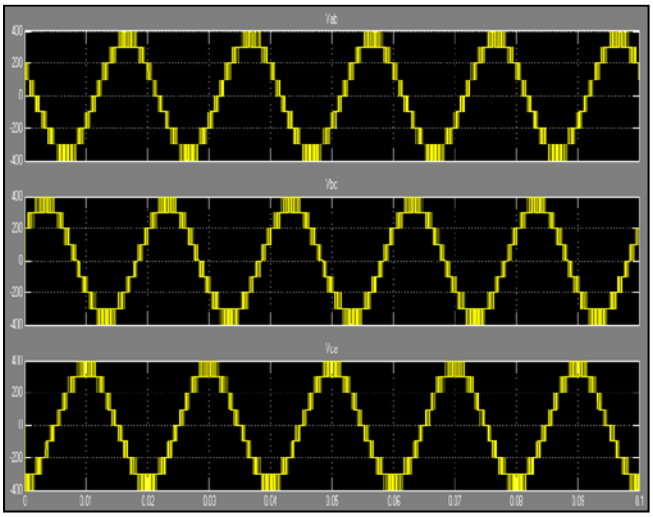
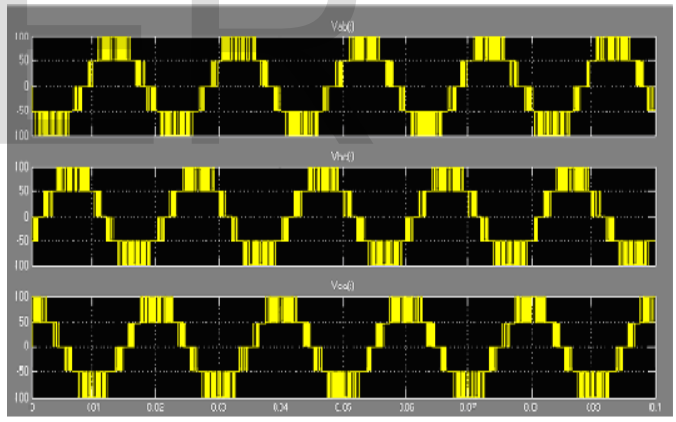


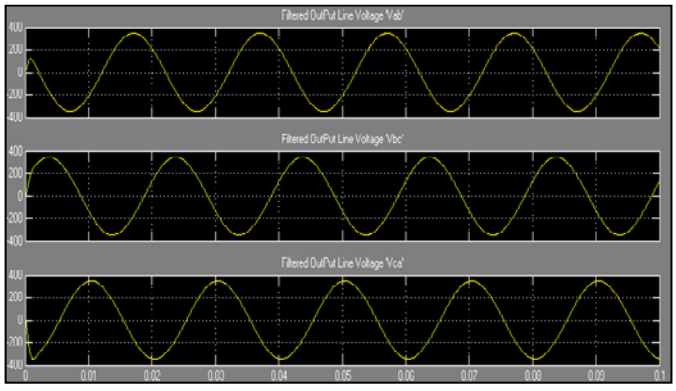
Fig. 5. The three output line voltages $V_{ab}(t)$, $V_{bc}(t)$ and $V_{ca}(t)$

The switching angles must be calculated in such a manner that the total harmonic distortion of the output voltage becomes as low as possible. In order to get low harmonic distortion in the output voltage, a proper method of harmonics elimination is used in which the switching angles are carefully calculated. Based on these calculations the lower dominant harmonics are eliminated easily. The Fourier analysis is necessary to be calculated to determine the frequency spectra of the output.

The output waveform of DCMLI consists of several steps of the DC voltages. The harmonics can also be eliminated by increasing the number of DC voltage levels in the output that adds up additional steps in the output. This creates a staircase output waveform which ultimately reaches to the desired waveform. Increased number of DC voltage levels (steps) results in reduction of the harmonic distortion to almost zero. This process of increasing the number of steps by increasing the number of DC voltage levels in the output waveform requires greater number of DC-link capacitors (DC voltage sources). Additional extra power switches leads to complexity of overall inverter structure and makes it more expensive. The line voltages ($V_{ab}(t)$, $V_{bc}(t)$ and $V_{ca}(t)$) contain some harmonic contents that are shown in Fig. 6-(a). When these line voltages are passed through a filter (lowpass second order LC network) much better results are obtained. This results in output line voltages which are pure sinusoidal. The filtered line voltages V_{ab}, V_{bc} and V_{ca} can be easily visualized in Fig. 6-(b).



(a)



(b)

Fig. 6. Output line voltages (a) unfiltered (b) filtered

4 CONCLUSION

Multilevel diode clamped inverters are the most favorable inverters for high and medium power. The newly introduced technique namely sinusoidal pulse width modulation (SPWM) is successfully validated for performance enhancement of multilevel inverters. Using this technique hormanic distortin is eliminated to great extent and the modulation index is observed as nearer to ”1”. The output voltage of the designed inverter is pure sinusoidal.

The issue of imbalance voltages due to DC-link capacitors is also properly addressed in this work using the same scheme of SPWM. The proposed 3-phase 5-level diode clamped multilevel inverter (DCMLI) has more stable and pure sinusoidal output line voltages as compared to other schemes for same inverters.

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